What is claimed is:

SUB A9

1. A method for reducing light reflectance in a photolithographic process, the method comprising the steps of:

providing a substrate having an inter-metal dielectric (IMD) layer on top including at least one via opening extending substantially perpendicular to a thickness therethrough; and

conformally depositing an anti-reflectance coating (ARC) layer over said IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening to reduce light reflectance.

2. The method according to claim 1, wherein prior to the step of conformally depositing an ARC layer an etching stop layer is formed over said IMD layer, and a first anti-reflectance coating (ARC) layer is formed over said etching stop layer.

3. The method of claim 2, wherein the etching stop layer comprises silicon oxynitride.

4. The method of claim 1, wherein the ARC layer comprises silicon oxynitride.

5. The method of claim 2, wherein the ARC layer comprises silicon oxynitride.

6. The method of claim 2, wherein the etching stop layer comprises silicon nitride.

7. The method of claim 1, wherein the ARC layer is selected from the group consisting of at least one of silicon oxynitride and titanium nitride.

8. The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. The method of claim 1, further comprising a subsequent photolithographic process including formation of trench openings substantially over the at least one via opening.

10. The method of claim 1, wherein said at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. A method of reducing an undercutting effect in a photoresist layer in a photolithographic process comprising the steps of:

providing a substrate having an inter-metal dielectric (IMD) layer on top, said IMD layer further comprising via openings extending through said IMD layer;

conformally forming an anti-reflectance coating (ARC) layer over said IMD layer and said via openings; and

forming a photoresist layer over said IMD layer and photolithographically exposing a pattern defining trench openings disposed at least partially over said via openings.

12. The method of claim 11, wherein the ARC layer comprises a second ARC layer conformally formed at least partially over a first ARC layer following formation of said via openings, said first ARC layer having been formed over the IMD layer prior to formation of said via openings.

13. The method of claim 11, wherein prior to forming the ARC layer, an etching stop layer is formed over the IMD layer.

14. The method of claim 13, wherein the etching stop layer comprises silicon oxynitride.

15. The method of claim 11, wherein the ARC layer is selected from the group consisting of at least one of silicon oxynitride and titanium nitride.

16. The method of claim 12, wherein the ARC layer comprises silicon oxynitride.

17. The method of claim 11, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. The method of claim 11, wherein said via openings are formed substantially adjacent to one another.

19. The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. A improved method of reducing light reflectance in a dual damascene structure, the method comprising the steps of:

forming a first dielectric layer on an underlying substrate;

forming at least one dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening substantially through the ARC layer, the at least one dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and

exposing selected regions of the layer of photoresist layer to light such that the light penetrates the layer of photoresist and is at least partially absorbed by the at least one additional ARC layer and the at least one ARC layer.

Add A10